# ne<mark>x</mark>peria

### Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <u>http://www.nxp.com</u>, <u>http://www.philips.com/</u> or <u>http://www.semiconductors.philips.com/</u>, use <u>http://www.nexperia.com</u>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © Nexperia B.V. (year). All rights reserved.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

## Ground and V<sub>CC</sub> Bounce of High-Speed Integrated Circuits

AN223

### Author: Mike Stevens

### INTRODUCTION

The purpose of this paper is to give a general description of what ground and  $V_{CC}$  bounce are, why it is they are tested, and a detailed description of how they are tested.

### WHY SHOULD GROUND AND V<sub>CC</sub> **BOUNCE BE TESTED?**

Ground and V<sub>CC</sub> bounce testing is done to evaluate what effect switching more than one output simultaneously has on the performance of the integrated circuit. This effect becomes important in any high-performance line of circuits because the propagation delays and output edge rates are very fast. This can cause ground bounce and V<sub>CC</sub> bounce, described as Voltage Output Low Peak (VOLP) and Voltage Output High Valley (V<sub>OHV</sub>), respectively.

Fast edge rates of the output drivers can team up with internal parasitic lead inductance and the output load to produce unwanted side effects of noise on the outputs. This noise or ringing will occur on both a static and a switching output. This ringing can be substantial enough to cross the input triggering threshold of a subsequent device, which in turn can cause a system to perform unpredictably and unreliably.

### GENERAL CONSIDERATIONS

There are two factors to consider when testing ground and V<sub>CC</sub> bounce: the test fixture and test methods. Both are of equal importance for accuracy, repeatability, and correlation.

These tests determine the magnitude of the peaks and valleys on the low and high static output levels during multiple output switching. VOHV refers to the minimum voltage "valley" on an output in the high level state. VOLP refers to the maximum voltage "peak" on an output in the low level state. Figure 1 shows a typical example of what  $V_{OLP}$  and  $V_{OHV}$  look like, and also defines the points where VOLP and VOHV are measured.

For circuits with a single output or a single complementary output, the circuit is set up so that the pin under test is switching and the VOLP and VOHV levels are then measured at the points on the waveform as shown in Figure 1.

The most accurate way to determine the actual voltage dropped across the package lead inductance is to measure the magnitude of the ringing while the tested output is in the steady state. To evaluate the worst case, the V<sub>CC</sub> should be at the maximum operating range, usually 5.5V, which will produce the highest V<sub>OH</sub> levels. The higher V<sub>OH</sub> level will create more dynamic switching current to

flow through the lead inductance and produce a larger voltage ring on the outputs.

For further information see references.

### GROUND BOUNCE METHOD

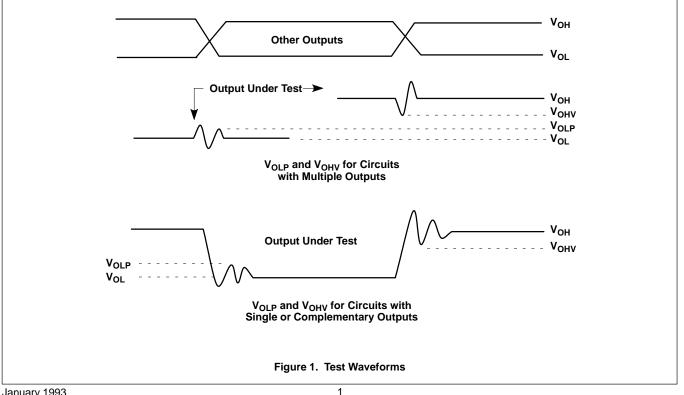
 $V_{OLP}$  is usually evaluated on the output pin furthest from the ground pin with the longest package lead length. The static output is in the low state and the switching outputs going from high to low. Examine the waveform and record the level of VOLP as defined by Figure 1.

VOLP should not be evaluated on the output adjacent to the ground pin. Mutual lead inductance will effectively reduce the magnitude of the output ringing by a factor of two.

### V<sub>CC</sub> BOUNCE METHOD

VOHV is usually evaluated on the output pin furthest from the  $V_{CC}$  pin with the longest package lead length. The static output is in the high state and the switching outputs going from low to high. Examine the waveform and record the level of V<sub>OHV</sub> as defined by Figure 1.

VOHV should not be evaluated on the output adjacent to the ground pin. Mutual lead inductance will effectively reduce the magnitude of the output ringing by a factor of two.



Application Note

### AN223

### VOLP VS. VIN METHOD

Set up the V<sub>OLP</sub> test and sweep the static input from 0.0V to 1.5V in 100mV increments, taking measurements at each point. Comparison data can be taken on a variety of ICs using the same set-up and test fixture. Plotting this data in graph form will show how the ICs compare with each other for input noise sensitivity during simultaneous switching. The same test can be performed on V<sub>CC</sub> bounce.

# TEST FIXTURES AND SET UP PROCEDURES

Refer to Table 1 for a complete list of test equipment and hardware. The test fixture will be the same one used for standard AC testing. This is a high-frequency PC board fixture featuring adequate internal ground and  $V_{CC}$  planes as well as 50 $\Omega$  micro strip line for all signal paths and close proximity loading. The test fixture should have  $V_{CC}$  decoupling of at least 100µF, 0.1µF, 0.01µF and 1000pF. For a complete discussion of fixturing requirements including grounding, bypassing and general high-frequency testing requirements refer to the Application Note entitled "Testing and Specifying FAST Logic" (FAST Data Manual: AN202) and "Printed Circuit Board Test Fixtures for High-Speed Logic" (ABT Data Manual: AN602).

### Pulse Generator Set Up

(Refer to "Test Circuit and Waveforms" in the appropriate data book for voltage levels and edge rates.)

Voltage levels:  $V_{IH}$ =3.0V,  $V_{IL}$ =0.0V Threshold voltage levels:  $V_{IH}$ =2.5V,  $V_{IL}$ =0.5V Rise and fall times: ( $t_R/t_F$ ) = 2.5ns (10% to 90%) Frequency: 1MHz @ 50% duty cycle The pulse generator should be set up to provide simultaneous switching of the input signals. ("Simultaneous" is defined as all the input pins of the device seeing a given signal at the same moment in time.)

The preferred method is to drive each input with a separate pulse generator channel. Each input signal should be terminated with  $50\Omega$  resistor as close to the input pin as possible. The Tektronix HFS9009 data generator provides channel delays with 1ps resolution on the edge placement accuracy. The input skew from channel to channel should be set up with a maximum limit of  $\pm$ 50ps, but the target is less than  $\pm$ 30ps. The greater the input skew is, the worse the correlation will be. For example, using ±100ps produces about 50mV error (5%) for  $V_{OLP}$  and  $\pm 250 ps$  produces about 100mV error (10%) for V<sub>OLP</sub>. Therefore, it becomes very important to use a tight input skew to produce accurate and repeatable data.

The second method is to use a ganged type configuration, where one pulse generator signal is used to drive all inputs. This method is employed when the number of device inputs exceeds the number of pulse generator channels. The input signal should be terminated with  $50\Omega$  and then branched out equally to all inputs needing the input signal. Line lengths from the termination to the device pin should be kept as short as possible and of equal lengths. The input edge rates should be as close as possible to the data manual specifications.

### **General Set Up**

All outputs should be loaded with the standard 50pF,  $500\Omega$  AC load.

When applicable, plots should be taken on at least one part and data values should be taken on three parts. The one part used for plots should have typical characteristics for the sample as a whole.

### V<sub>CC</sub> BOUNCE TESTING Voltage Output High Valley (V<sub>OHV</sub>)

Measure the V<sub>OHV</sub> level on an output held high during simultaneous switching. (Non-storage type devices only.)

The output to be evaluated for  $V_{OHV}$  should be the pin farthest from the  $V_{CC}$  pin. If there are two equidistant pins, record data on both outputs and plot only the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested. The output should be evaluated on the Low to High transition of the switching outputs.

- 1.  $V_{CC} = 5.5V$ , Temp =  $-55^{\circ}C$  and  $V_{CC} = 5.0V$ , Temp =  $25^{\circ}C$
- 2. Three parts are tested and plots should be taken on one of the parts.
- 3. The input conditions should be set so that the output under test is a static high.
- Switch the remaining outputs simultaneously from low to high and record V<sub>OHV</sub>.
- 5. Plot waveforms of a switching input, the high output, and a switching output.

Repeat steps 4 through 5 for the following other modes:

- High to Low
- 3-State to Low (if possible)
- Low to 3-State (if possible)
- High to 3-State (if possible)
- 3-State to High (if possible)

### GROUND BOUNCE TESTING Voltage Output Low Peak (V<sub>OLP</sub>)

Measure the  $V_{OLP}$  level on an output held low during simultaneous switching. (Non-storage type devices only.)

### Table 1. Equipment Requirements (Hardware)

DEVICE	CHARACTERISTICS	MODEL
Digital Oscilloscope	1GHz bandwidth, 50 $\Omega$ channels and cables	TEK11402
Data Generator	36 channel, 1ps edge placement resolution	TEK HFS9009
Temperature Forcing Unit	-55°C to +125°C (Thermonics)	T2420
Power Supply	4 channel, 0V–20V @ 5A	HP6632A
Test Fixture	High frequency (900MHz); Controlled 50 $\Omega$ impedance; Full ground and V <sub>CC</sub> planes; Sufficient V <sub>CC</sub> decoupling (Chip caps and Tantalum caps)	SIG SD8807.27

### Ground and V<sub>CC</sub> Bounce of High-Speed Integrated Circuits

### GROUND BOUNCE TESTING Voltage Output Low Peak (V<sub>OLP</sub>) (CONTINUED)

The output to be evaluated for  $V_{OLP}$  should be the pin farthest from the Ground pin. If there are two equidistant pins, record data on both outputs and plot only the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested. The output should be evaluated on the High to Low transition of the switching outputs.

- 1.  $V_{CC} = 5.5V$ , Temp =  $-55^{\circ}C$  $V_{CC} = 5.0V$ , Temp =  $25^{\circ}C$
- 2. Three parts are tested and plots should be taken on one of the parts.
- 3. The input conditions should be set so that the output under test is a static low.
- Switch the remaining outputs simultaneously from high to low and record V<sub>OLP</sub>.
- 5. Plot waveforms of a switching input, the low output, and a switching output.

Repeat steps 4 through 5 for the following other transitions:

- Low to High
- 3-State to Low (if possible)
- Low to 3-State (if possible)
- High to 3-State (if possible)
- 3-State to High (if possible)

#### NOISE IMMUNITY COMPARISON TESTING V<sub>OLP</sub> VS. V<sub>IN</sub>

Set up the  $V_{OLP}$  test and measure  $V_{OLP}$  while incriminating the static input voltage. (Non-storage type devices only).

The output to be evaluated for  $V_{OLP}$  should be the pin farthest from the ground pins. If there are two equidistant pins, record data on the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested. The output should be evaluated on the falling edge of the switching outputs.

- 1.  $V_{CC} = 5.5V$ , Temp =  $-55^{\circ}C$  and  $V_{CC} = 5.0V$ , Temp =  $25^{\circ}C$
- 2. One part of each variety to be tested.
- Evaluate V<sub>OLP</sub> while the other outputs switch simultaneously from high to low.
- 4. Increment V<sub>IN</sub> on the static input from 0.0V to 1.5V in 100mV increments and record V<sub>OLP</sub> at each increment. Graph data for all parts as V<sub>OLP</sub> vs. V<sub>IN</sub> (V<sub>IN</sub> on X axis, and V<sub>OLP</sub> on the Y axis). Use a power supply output to drive the static input.

As long as the testing set-up and the fixture are identical, this graph will show an accurate comparison of ground bounce sensitivity among the parts. (The same test can be performed on  $V_{OHV}$  by setting up the  $V_{OHV}$ 

test and sweeping the static input from 3.0V to 1.5V in 100mV increments.)

### REFERENCES

- Jeffrey A. West, "Mathematical Modeling of Ground Bounce Phenomenon," *Spice Simulation Design Guide*, Orem, UT: Signetics Corp., December 1990.
- "Package Lead Inductance Considerations in High-Speed Applications" (AN212), FAST Data Manual, Sunnyvale, CA: Signetics Corp., 1989.
- "ABT Bench Test/Characterization," *Philips Semiconductor Internal Document*, Sunnyvale, CA: Signetics Corp., 1992.
- "Simultaneous Switching Evaluation of Advanced CMOS Logic" (AN601), ACL Data Manual, Sunnyvale, CA: Signetics Corp., 1989.
- "Testing and Specifying FAST Logic" (AN202), FAST Data Manual, Sunnyvale, CA: Signetics Corp., 1989.
- "Test Fixtures for High-Speed Logic" (AN203), FAST Data Manual, Sunnyvale, CA: Signetics Corp., 1989.
- "Printed Circuit Board Test Fixtures for High-Speed Logic" (AN602), ABT Data Manual, Sunnyvale, CA: Signetics Corp., 1991.

AN223